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L8: Entry 2 of 10 File: USPT May 6, 2003

DOCUMENT-IDENTIFIER: US 6560756 B1
TITLE: Method and apparatus for distributed test pattern decompression

CLAIMS:

26. A method comprising: a) writing, within different memories, compressed versions of the same relative section for each of a plurality of different Device Under Test (DUT) connections; b) reading, from said memories, said compressed versions of the same relative section for each of a plurality of different test patterns; c) decompressing each of said sections with different decompression engines to form decompressed versions of the same relative section for each of a plurality of different test patterns; and d) writing, back into their respective memories, said decompressed versions of the same relative section for each of a plurality of different DUT connections.

L8: Entry 6 of 10 File: USPT Feb 10, 1987

DOCUMENT-IDENTIFIER: US 4642784 A
**** See image for Certificate of Correction ****
TITLE: Integrated circuit manufacture

CLAIMS:

14. A method of determining the causes of failures of semiconductor devices which are known to have fault areas, said areas of the semiconductor devices having cells into which data is written and from which data is read, comprising the steps of:

subjecting each of said devices to a plurality of different sequences of electrical tests which have different patterns of data 1's and 0's written into said cells at a plurality of different patterns of addresses to produce a plurality of sets of pass/fail indicators for each device for a selected one of said fault areas; said pass/fail indicators being the results of said sequences of electrical tests;

comparing said plurality of sets of pass/fail indicators for said selected one of said fault areas for each said device to a catalog of sets of pass/fail indicators which are known to define unique failure causes, to determine matches.

L3: Entry 15 of 29 File: USPT Mar 24, 1998

DOCUMENT-IDENTIFIER: US 5732022 A
TITLE: Non-volatile semiconductor memory device

Brief Summary Text (2):
The present invention relates to a non-volatile semiconductor memory device, and more specifically to an electrically data rewritable non-volatile semiconductor memory device excellent in the data erasure characteristics, easy to test the overerasure status, and high in access speed.

CLAIMS:

1. A non-volatile semiconductor memory device, comprising:

a memory cell array composed of a plurality of electrically data writable and erasable non-volatile memory cells arranged in a matrix pattern, each of the memory cells being a transistor having a source, a drain, a floating gate and a control gate; data being written in each memory cell by injecting electrons into the floating gate thereof and erased from each memory cell by extracting electrons from the floating gate thereof; said drain of each memory cell being connected to a bit-line which receives data from the memory cell, a test of data erasure being achieved by checking whether the source-drain can be turned on or not when a predetermined voltage is kept applied to the control gate, turning on or not of said memory cell being checked based on the potential of the bit-line, the bit-line being connected to an I/O pad when the test of data erasure is achieved so that the potential of the bit-line may be measured external to the memory device; and

a source bias circuit for applying a positive bias voltage to the sources of the memory cells to be tested in the erasure test, to shift each threshold value of each memory cell in a forward direction thereof, said positive bias voltage being a variable voltage that is externally applied to the memory device.

L3: Entry 16 of 29 File: USPT Mar 3, 1998

DOCUMENT-IDENTIFIER: US 5724289 A
TITLE: Nonvolatile semiconductor memory capable of selectively performing a pre-conditioning of threshold voltage before an erase self-test of memory cells and a method related therewith

Brief Summary Text (3):
The present invention relates generally to a non-volatile semiconductor memory and a test method for the memory, and more particularly to a flash memory formed of an electrically data writable and all data erasable read only memory in which a self-test function is provided and a charge injection is performed before all data erasure to equalize threshold values of memory cells with each other.

L8: Entry 1 of 10 File: USPT Oct 7, 2003

DOCUMENT-IDENTIFIER: US 6631340 B2
TITLE: Application specific event based semiconductor memory test system

Abstract Text (1):
A semiconductor test system for testing semiconductor devices has a plurality of different tester modules and an algorithmic pattern generator (ALPG) for generating an algorithmic pattern specific to an intended memory, thereby achieving a low cost and application specific memory test system. The semiconductor test system includes two or more tester modules whose performances are different from one another, an ALPG module for generating an algorithmic pattern which is specific to the memory, a test system main frame to accommodate a combination of the tester modules and the ALPG module, a test fixture for electrically connecting the tester modules and a device under test, a performance board provided on the test fixture for mounting the device under test, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus.